WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

providing a semiconductor substrate having a first conductivity type and having a first impurity concentration at a whole of a principal surface of said semiconductor substrate;

forming an epitaxial layer of said first conductivity type on said principal surface;

forming a well region of said first conductivity type in said epitaxial layer by introducing an impurity in said epitaxial layer through a surface of said epitaxial layer;

forming a gate oxide film on a surface of said epitaxial layer;

forming a gate electrode on said gate oxide film on said well region;

forming semiconductor regions in said epitaxial layer serving as a source region and a drain region; and

forming a capacitor element electrically coupled to one of said semiconductor regions,

wherein an impurity concentration of said well region is greater than both an impurity concentration of said epitaxial layer and said first impurity concentration.

2. A method of manufacturing a semiconductor integrated circuit device according to claim 1, wherein said epitaxial layer has substantially a same impurity concentration as a designed impurity concentration of said first impurity concentration.

3. A method of manufacturing a semiconductor integrated circuit device according to claim 1, wherein an impurity concentration of said semiconductor substrate is about 10^{15} atoms/cm^3.

4. A method of manufacturing a semiconductor integrated circuit device according to claim 3, wherein a thickness of said epitaxial layer is within a range of 0.3μm to 5μm.

5. A method of manufacturing a semiconductor integrated circuit device according to claim 3, wherein said well region extends into said semiconductor substrate, such that an impurity concentration of said well region gradually decreases from said epitaxial layer into said semiconductor substrate through an interface portion therebetween.

6. A method of manufacturing a semiconductor integrated circuit device according to claim 1, wherein a thickness of said epitaxial layer is within a range of 0.3μm to 5μm.

7. A method of manufacturing a semiconductor integrated circuit device according to claim 1, wherein a memory cell of a dynamic random access memory includes said capacitor element and a MISFET comprising said gate insulating film, said gate electrode, and said semiconductor regions.

8. A method of manufacturing a semiconductor integrated circuit device according to claim 7, wherein said semiconductor substrate is a relatively lightly doped semiconductor substrate.

9. A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

forming an epitaxial layer of a first conductivity type on a semiconductor substrate having a first conductivity type and having a first impurity concentration at a whole of said principal surface of said semiconductor substrate, such that said epitaxial layer is formed on said principal surface of said first

impurity concentration, wherein a thickness of said epitaxial layer is within a range of 0.3μm to 5μm;

forming a well region in said epitaxial layer by introducing an impurity in said epitaxial layer through a surface of said epitaxial layer;

forming a gate oxide film of an MISFET on a surface of said epitaxial layer;

forming a gate electrode of said MISFET on said gate oxide film on said well region;

forming semiconductor regions in said epitaxial layer serving as a source region and a drain region of said MISFET; and

forming a capacitor element electrically coupled to one of said semiconductor regions,

wherein said first impurity concentration is lower than an impurity concentration of a portion of said well region where a channel region of said MISFET is formed.

10. A method of manufacturing a semiconductor integrated circuit device according to claim 9, wherein said epitaxial layer has substantially a same impurity concentration as a designed impurity concentration of said first impurity concentration.

11. A method of manufacturing a semiconductor integrated circuit device according to claim 9, wherein a memory cell of a dynamic random access memory comprises said MISFET and said capacitor element.